Instruction Manual

Tektronix

TMS711
320C6211/C6711 Microprocessor Support

071-0877-00

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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Table of Contents

List of Figures

List of Tables

General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Preface

This instruction manual contains specific information about the TMS711 320C6211/C6711 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS711 320C6211/C6711 support was purchased, you will only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support. See Manual Conventions below for more information.

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a user manual covering the basic operations of microprocessor support.

Contacting Tektronix

Phone	1-800-833-9200*
Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 1-503-627-2400 6:00 a.m. – 5:00 p.m. Pacific time

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This chapter contains information on the TMS711 320C6211/C6711 microprocessor support package, and information on connecting your logic analyzer to your system under test.

Support Package Description

The TMS711 320C6211/C6711microprocessor support package displays disassembled data from systems based on the Texas Instruments C6211/C6711 microprocessor.

To use this support efficiently, you need to have the items listed in the information on basic operations and the following documents:

- *TMS320C6000 CPU and Instruction Set Reference Guide*, Literature Number: SPRU189D, March 1999.
- *TMS320C6000 Peripheral Reference Guide*, Literature Number: SPRU190C, April 1999.
- *TMS320C6000 EMIF to External SDRAM/SGRAM Interface*, Literature Number: SPRA433A, June 1999.
- *TMS320C6000 EMIF to External SBSRAM Interface*, Literature Number: SPRA533A, April 1999.
- *TMS320C6000 Digital Signal Processor Data Sheet*, Literature Number: SPRS073, March 1999.
- *TMS320C6000 EMIF to External Asynchronous SRAM Interface*, Literature Number: SPRA542, April 1999.

Information on basic operations also contains a general description of support.

Logic Analyzer Software Compatibility

The floppy disk label on the microprocessor support states which version of logic analyzer software this support is compatible with.

Logic Analyzer Configuration

The TMS711 320C6211/C6711support requires a minimum of one 102-channel module.

***NOTE**. It is recommended that a logic analyzer acquisition module with a maximum bus speed of 100 MHz be required when ECLKOUT = 100 MHz (maximum). For ECLKOUT above 100 MHz (maximum), a logic analyzer acquisition module with a maximum bus speed of 200 MHz is required.*

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor support packages in the information on basic operations as they pertain to your system under test.

You should also review electrical, environmental, and mechanical specifications in *Specifications* on page 3–1 as they pertain to your system under test, as well as the following descriptions of other C6211/C6711 support requirements and restrictions.

System Clock Rate

The operating speeds that the C6211/C6711 support can acquire data from the C6211/C6711 microprocessor are listed on Table 3–1. These specification were valid at the time this manual was printed. Please contact your Tektronix Sales Representative for current information on the fastest devices supported.

NonIntrusive Acquisition

Acquiring microprocessor bus cycles will be non intrusive to the system under test. That is, the C6211/C6711 support will not intercept, modify, or present signals back to the system under test.

Disabling the Instruction Cache

To display disassembled acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus they then can be acquired and displayed disassembled.

L2 Cache

Do not configure L2 cache as cache; or external memory bus cycle acquisitions will not occur with L2 cache.

Write Cycle

SBSRAM Write Cycle and SDRAM Write Cycle have the same control values, so they are represented by a single name. For example SDWRITE/SBSWRITE for a given sequence in the control column, but the corresponding mnemonic

column will have clear cut labels, for example (SDRAM WRITE CYCLE) and (SBSRAM WRITE CYCLE).

Read Cycle SBSRAM Read Cycle and SDRAM Read Cycle have same control values, so they are represented by a single name. For example SDREAD/SBSREAD for a given sequence in the control column, but the corresponding mnemonic column will have clear cut labels, for example (SDRAM READ CYCLE) and (SBSRAM READ CYCLE).

Opcode Fetch/Data Read. The C6211/C6711 support does not provide a signal to distinguish between Data Read and Opcode Fetch. The TMS711 320C6211/C6711 support makes a reasonable estimate at looking at the address values of a few sequences around the current sequence or by looking at the processor signal. Yet, in some instances you may need to use the Mark Opcode function.

Symbol 11111[bin] The Control symbol table does not have a symbol for 11111[bin], since it can mean SDRAM Read, Write, or Fetch.

Conditional Branches Flushes cannot be shown for conditional branches (where Condition is True) when the branch instruction is in the first fetch packet, and the target address is in third and fourth fetch packet from the fetch packet which has Branch instructions (in either forward or reverse branches).

Alternate Fetch Packet If a conditional branch instruction is in the fetch packet, and the target address is in the alternate fetch packet (from the fetch packet which has the branch instruction; for example 1 to 3 , 2 to 4, or 3 to 5) we do not show flushes, since fetch packets appear in sequence.

Branch Instructions For branch instructions (both conditional and unconditional): B.S2 IRP, B.S2 NRP and B.S2 src2reg, we do not show whether a branch was taken or not in the listing window of our disassembly. Since we cannot get the contents of the registers IRP, NRP, Bxx that have the target address.

Memory Types The C6211/C6711 support disassembles the execution from any one of the memory types: SDRAM, SBSRAM, and ASYNC, at a time.

SBSRAM 4 SBSRAM 4 word burst Read and write cycles are supported. But SBSRAM 6 word burst Read and write cycles not supported due to timing considerations.

Memory-Space Signals All Memory space signals CE[3–0]~ must be connected to the logic analyzer.

External Memory In the C6211 external memory you can download the C6211/C6711 support programs only at addresses in multiples of 0x20; for example, 80000000, 80000020,80000040. Hence, the user input fields for entering the start address of the Interrupt-Service-Fetch packets must be appropriate.

Functionality Not Supported

Microprocessor The signals: HPI, MCBSP 0 & 1, and JTAG are not acquired. If you want to view these signals, you need to find an alternate way to probe them.

Alternate Bus master Alternative bus master transactions are acquired by the C6211/C6711 support and are not disassembled.

Features not Tested

The C6211/C6711 support has been tested for C6711 floating point instructions by editing the refmem. The C6211/C6711 support is not evaluated by acquiring cycles from a dedicated C6711 evaluation board.

The C6211/C6711 support disassembles SDRAM, SBSRAM and ASYNC memory cycles. The C6211/C6711 support is not tested for SBSRAM and ASYNC cycles. This C6211/C6711 support has been tested only with 32bit SDRAM cycles.

The C6211/C6711 support has not been tested for Interrupts.

The C6211/C6711 support has not been tested for Big Endian mode.

Miscellaneous

The Address shown for the SDRAM ACTV cycle is the row address for the corresponding user input for the SDRAM Address Configuration.

Connecting the Logic Analyzer to a System Under Test

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your system under test.

To connect the probes to C6211/C6711 signals in the system under test using a test clip, follow these steps:

1. Turn off power to your system under test. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, and the logic analyzer module. To prevent static damage, handle these components only in a static-free environment.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from the test clip.

CAUTION. *Failure to place the system under test on a horizontal surface before connecting the test clip can permanently damage the pins on the microprocessor.*

3. Place the system under test on a horizontal static-free surface.
4. Use Tables 5–2 through 5–16 beginning on page 5–3 to connect the channel probes to C6211/C6711 signal pins on the test clip or in the system under test.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Operating Basics

Setting Up the Support

The information in this section is specific to the operations and functions of the TMS711 320C6211/C6711 microprocessor support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and display disassembled data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The microprocessor support provides default values for each of these setups as well as user-definable settings.

Installing the Support Software

NOTE. *Before you install any software, it is recommended you verify that the microprocessor support software is compatible with the logic analyzer software.*

To install the TMS711 320C6211/C6711 software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software, follow the above instructions and select Uninstall. You must close all windows before you uninstall any software.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the TMS711 320C6211/C6711 support are Address, Data, Control, Async, CEnable, BEnable, and Misc. The channel groups tables begin on page 5–1.

Support Package Setups

The TMS711 320C6211/C6711 software installs C6211 support package setup file.

C6211 Setup

This setup provides disassembly support. All signals are not inverted and displayed as they appear electrically on the front side bus.

Disassembly channel groups:

Address	Data	Async	CEnable
BEnable	Misc		

Clocking

Options

The TMS711 320C6211/C6711support offers a microprocessor-specific clocking mode for the C6211/C6711 microprocessor. This clocking mode is the default selection whenever you load the TMS711 320C6211/C6711 support.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes in more detail how to use these clock selections for general purpose analysis.

- Internal clocking is used for timing and is based on the clock generated by a Tektronix logic analyzer. You can configure the clock rate from 50 ms down to 4 ns resolution.
- External clocking is used when you configure the clocking of data based on logical combinations of clocks and qualifiers.

Custom Clocking

When Custom is selected, the Custom Clocking Options menu will have the subtitle C6211 Microprocessor Clocking Support added, and the clocking options will also be displayed.

The TMS711 320C6211/C6711support has three clock state machines (CSM). There is one select field with the label Memory Type: that field will contain the following selections: ASYNC, SBSRAM, and SDRAM.

Memory operation type:

ASYNC	Selects CSM for ASYNC	(default)
SBSRAM	Selects CSM for SBSRAM	
SDRAM	Selects CSM for SDRAM	

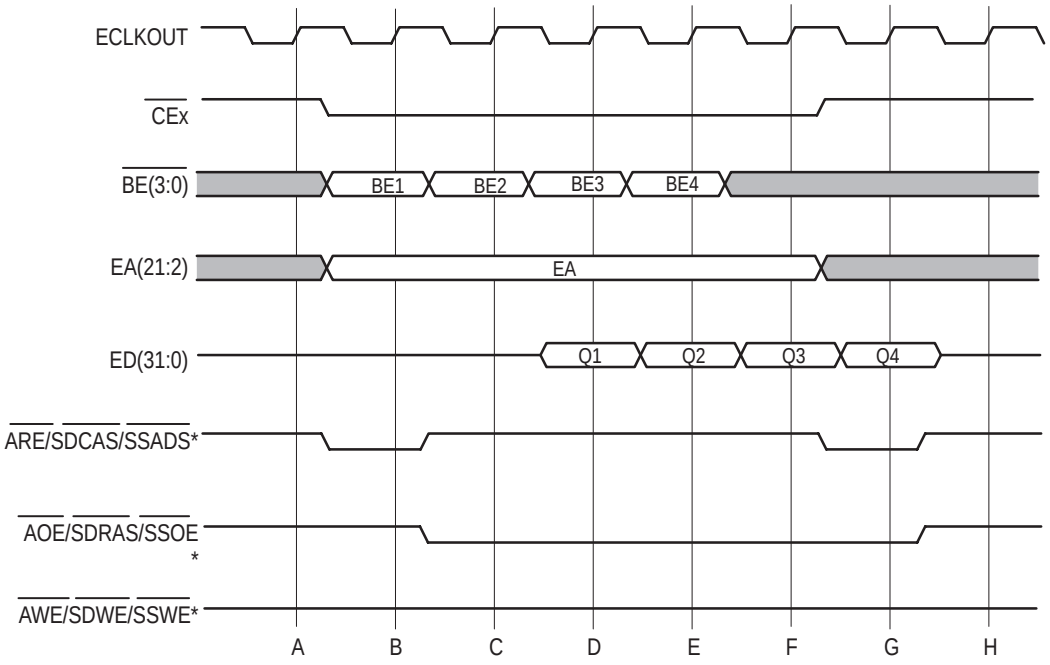
CAS Latency. Choose this field for only SDRAM Clocking state machine. There are two options:

Two	Choose for CAS latency two
Three	Choose for CAS latency three

Setup and Hold Time. The user can change the Setup and Hold time window of all the signal groups. The default Setup time is 2.5 ns and the Hold time is 0 ns. The user defined Setup and Hold will have precedence over any default Setup and Hold time.

***NOTE**. The signals present in the Async group are also present in the Control group. The Setup and Hold values entered for the first one of those groups are used for all instances of that channel in the other groups.*

Figures 2–1 through 2–6 illustrate the bus timing for the SBSRAM, ASYNC, and SDRAM memory operations. The Custom Clock is the rising edge of the ECLKOUT.



Note: *ARE/SDCAS/SSADS, AOE/SDRAS/SSOE and AWE/SDWE/SSWE operate as SSADS, SSOE and SSWE, respectively, during SBSRAM accesses.

Figure 2–1: Bus timing for the SBSRAM Read cycle with a burst of four data transitions

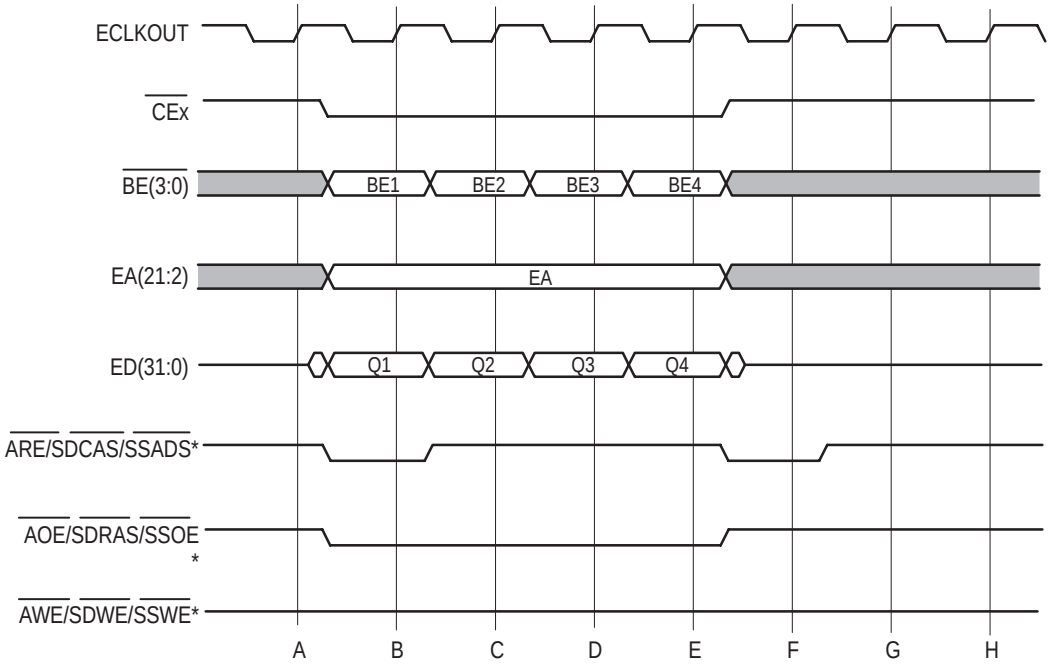
Table 2–1: Signal acquisition in SBSRAM Read cycle

Qualifiers		Operation	Signals	Custom Clock
ARE~/SDCAS~/SSADS~	= LOW	Sample and Master	CEx~, BE1, EA[21:2]	At position B
AOE~/SDRAS~/SSOE~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			
ARE~/SDCAS~/SSADS~	= HIGH	Sample and Master	BE2	At position C
AOE~/SDRAS~/SSOE~	= LOW			
AWE~/SDWE~/SSWE~	= HIGH			
ARE~/SDCAS~/SSADS~	= HIGH	Sample and Master	BE3, Q1	At position D
AOE~/SDRAS~/SSOE~	= LOW			
AWE~/SDWE~/SSWE~	= HIGH			

Table 2–1: Signal acquisition in SBSRAM Read cycle (Cont.)

Qualifiers		Operation	Signals	Custom Clock
ARE~/SDCAS~/SSADS~	= HIGH	Sample and Master	BE4, Q2	At position E
AOE~/SDRAS~/SSOE~	= LOW			
AWE~/SDWE~/SSWE~	= HIGH			
ARE~/SDCAS~/SSADS~	= HIGH	Sample and Master	Q3	At position F
AOE~/SDRAS~/SSOE~	= LOW			
AWE~/SDWE~/SSWE~	= HIGH			
ARE~/SDCAS~/SSADS~	= LOW	Sample and Master	Q4	At position G
AOE~/SDRAS~/SSOE~	= LOW			
AWE~/SDWE~/SSWE~	= HIGH			

Figure 2–2 shows the bus timing for the SBSRAM Write cycle with a burst of 4 data transitions.



Note: *ARE/SDCAS/SSADS, AOE/SDRAS/SSOE and AWE/SDWE/SSWE operate as SSADS, SSOE and SSWE, respectively, during SBSRAM accesses.

Figure 2–2: SDSRAM Write cycles with a burst of four data transitions

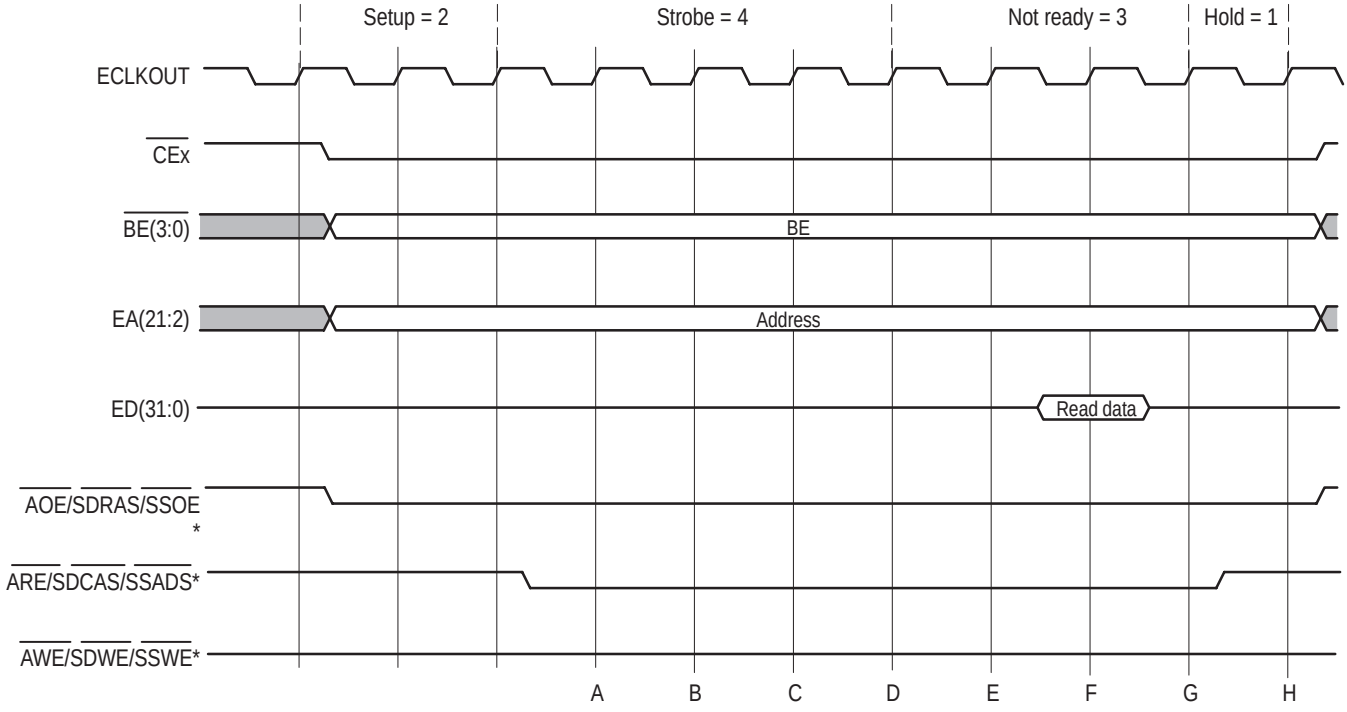
Table 2–2: Signal acquisition in SBSRAM Write cycle

Qualifiers		Operation	Signals	Custom Clock
ARE~/SDCAS~/SSAD~	= LOW	Sample and Master	CEx~, BE1, EA[21:2], and Q1	At position B
AOE~/SDRAS~/SSOE~	= HIGH			
AWE~/SDWE~/SSWE~	= LOW			
ARE~/SDCAS~/SSADS~	= HIGH	Sample and Master	BE2, Q2	At position C
AOE~/SDRAS~/SSOE~	= HIGH			
AWE~/SDWE~/SSWE~	= LOW			
ARE~/SDCAS~/SSADS~	= HIGH	Sample and Master	BE3, Q3	At position D
AOE~/SDRAS~/SSOE~	= HIGH			
AWE~/SDWE~/SSWE~	= LOW			

Table 2–2: Signal acquisition in SBSRAM Write cycle (Cont.)

Qualifiers		Operation	Signals	Custom Clock
ARE~/SDCAS~/SSADS~	= HIGH	Sample and Master	BE4, Q4	At position E
AOE~/SDRAS~/SSOE~	= HIGH			
AWE~/SDWE~/SSWE~	= LOW			
ARE~/SDCAS~/SSADS~	= LOW	Come out of the loop	——	At position F
AOE~/SDRAS~/SSOE~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			

Figure 2–3 shows the bus timing for the ASYNC Read cycle memory operations.



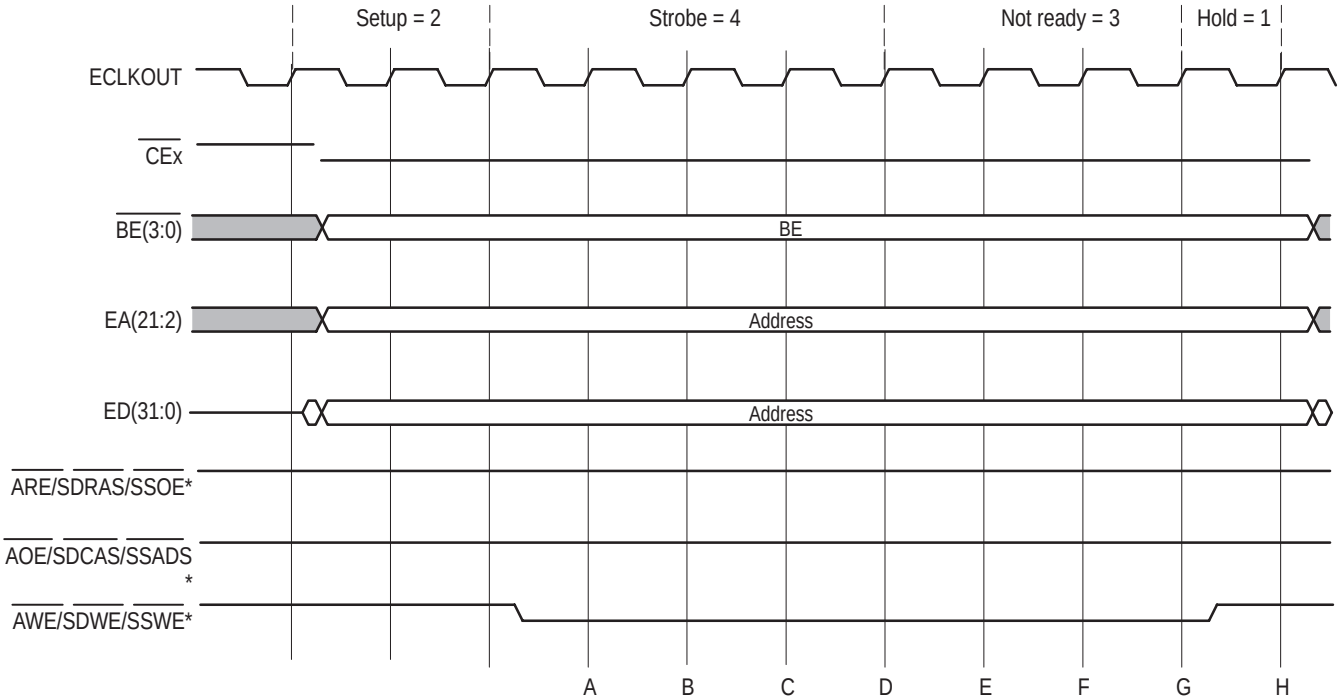
Note: *ARE/SDCAS/SSADS, AOE/SDRAS/SSOE and AWE/SDWE/SSWE operate as ARE, AOE and AWE, during ASYNC accesses. Data group is delated by 1 Clock.

Figure 2–3: Bus timing for the ASYNC read cycle

Table 2–3: Signal acquisition in ASYNC Write cycle

Qualifiers		Operation	Signals	Custom Clock
AOE~/SDRAS~/SSOE~	= LOW	Sample	CEx~, BE, Address, and Data	At positions A to G
ARE~/SDCAS~/SSADS~	= LOW			
AWE~/SDWE~/SSWE~	= HIGH			
AOE~/SDRAS~/SSOE~	= LOW	Master	The signals sampled at position G	At position H
ARE~/SDCAS~/SSADS~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			

Figure 2–4 shows the bus timing for the ASYNC Write cycle memory operations.



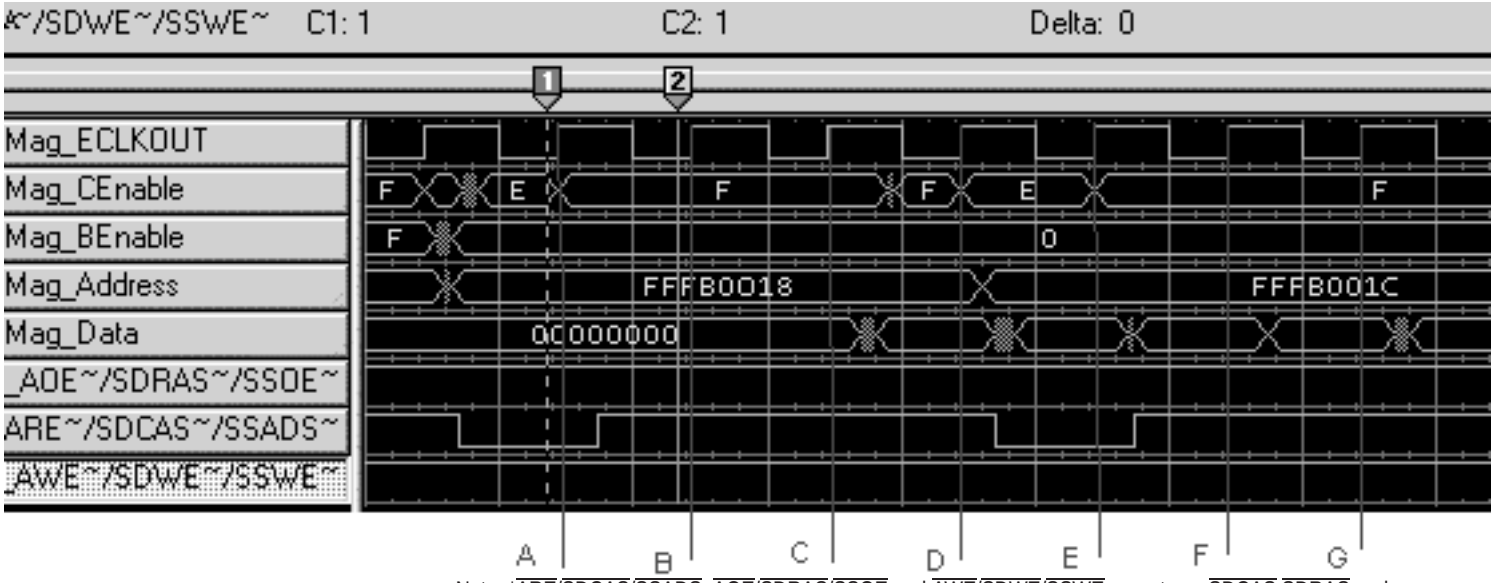
Note: *ARE/SDCAS/SSADS, AOE/SDRAS/SSOE and AWE/SDWE/SSWE operate as ARE, AOE and AWE, during ASYNC accesses.

Figure 2–4: Bus timing for the ASYNC write cycle

Table 2–4: Signal acquisition in ASYNC Write cycle

Qualifiers		Operation	Signals	Custom Clock
AOE~/SDRAS~/SSOE~	= HIGH	Sample	CEx~, BE, Address, and Data	At positions A to G
ARE~/SDCAS~/SSADS~	= HIGH			
AWE~/SDWE~/SSWE~	= LOW			
AOE~/SDRAS~/SSOE~	= HIGH	Master	The signals sampled at position G	At position H
ARE~/SDCAS~/SSADS~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			

Figure 2–5 shows a SDRAM Fetch cycle with CAS latency = 3.



Note: *ARE/SDCAS/SSADS, AOE/SDRAS/SSOE and AWE/SDWE/SSWE operate as SDCAS SDRAS and SDWE, during SDRAM accesses.

Figure 2–5: Bus timing for the SDRAM fetch cycle with CAS latency of 3

Table 2–5: Signal acquisition in SDRAM fetch cycle with CAS latency of 3

Qualifiers		Operation	Signals	Custom Clock
AOE~/SDRAS~/SSOE~	= HIGH	Sample and Master	CEnable, Address, Qualifiers	At position A
ARE~/SDCAS~/SSADS~	= LOW			
AWE~/SDWE~/SSWE~	= HIGH			
AOE~/SDRAS~/SSOE~	= HIGH	Sample and Master	BE1, CEnable, Address, Qualifiers	At position B
ARE~/SDCAS~/SSADS~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			
AOE~/SDRAS~/SSOE~	= HIGH	Sample and Master	BE2, CEnable, Address, Qualifiers	At position C
ARE~/SDCAS~/SSADS~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			
AOE~/SDRAS~/SSOE~	= HIGH	Sample and Master	BE3, Data 1, CEnable, Address, Qualifiers	At position D
ARE~/SDCAS~/SSADS~	= LOW			
AWE~/SDWE~/SSWE~	= HIGH			
AOE~/SDRAS~/SSOE~	= HIGH	Sample and Master	BE4, Data 2, CEnable, Address, Qualifiers	At position E
ARE~/SDCAS~/SSADS~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			
AOE~/SDRAS~/SSOE~	= HIGH	Sample and Master	Data 3 to Data 8, CEnable, Address, Qualifiers	At positions F to next 5 following clocks
ARE~/SDCAS~/SSADS~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			

***NOTE**. The default burst in the SDRAM Fetch cycle is 4, but since in Figure 2–5 ARE~/SDCASE~/SSADS~ asserts twice, 8 data transitions appear in the bursts. So this burst of data transitions was sampled and mastered. This is the timing cycle behavior usually seen on the logic analyzer.*

Figure 2–6 shows a SDRAM Write cycle with a default of four data transitions.

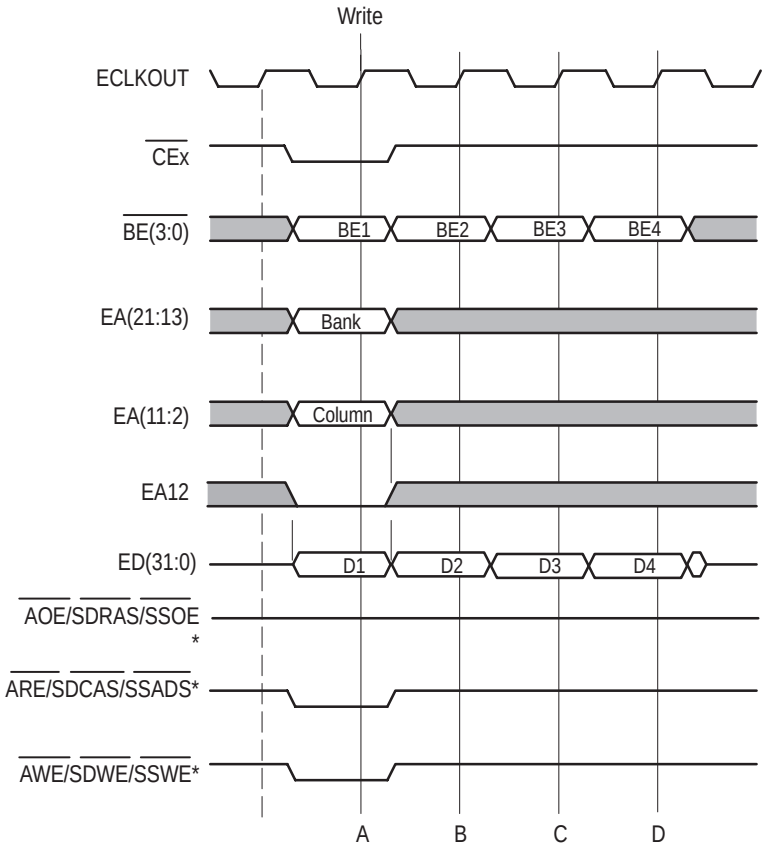


Figure 2–6: SDRAM Write cycle with default of four data transitions

Table 2–6: Signal acquisiton in SDRAM write cycle with CAS latency of 3

Qualifiers		Operation	Signals	Custom Clock
AOE~/SDRAS~/SSOE~	= HIGH	Sample and Master	CEnable, BE1, D1, Address,Qualifiers	At position A
ARE~/SDCAS~/SSADS~	= LOW			
AWE~/SDWE~/SSWE~	= LOW			
AOE~/SDRAS~/SSOE~	= HIGH	Sample and Master	BE2, D2	At position B
ARE~/SDCAS~/SSADS~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			
AOE~/SDRAS~/SSOE~	= HIGH	Sample and Master	BE3, D3	At position C
ARE~/SDCAS~/SSADS~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			
AOE~/SDRAS~/SSOE~	= HIGH	Sample and Master	BE4, D4	At position D
ARE~/SDCAS~/SSADS~	= HIGH			
AWE~/SDWE~/SSWE~	= HIGH			

Acquiring and Viewing Disassembled Data

Acquiring Data

Once you load the C6211/C6711 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in six display formats: Timing, State, Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE*. Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–16.*

The default display format displays the Address, Data, and Control channel group values for each sample of acquired data.

If a channel group is not visible, you must use the Disassembly property page to make the group visible.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–7 lists these special characters and strings and gives a definition of what they represent.

Table 2–7: Description of special characters in the display

Character or string displayed	Definition
>>	The instruction was manually marked.
t	Indicates the number shown is in decimal, such as #12t

Timing Display Format

The timing-waveform display format file is provided for the TLA 700 Series support. The timing-waveform display format file will set up and display the following waveforms:

Address	(busform)
Data	(busform)
ASYNC	(busform)
Control	(busform)
CEnable	(busform)
BEnable	(busform)
ECLKOUT	(busform)

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–8 lists cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–8: Cycle type definitions

Cycle Type	Definition
(RESET CYCLE)	Indicates system RESET
(ALTERNATE BUS MASTER CYCLE)	Indicates HOLD cycle
(SDRAM DEAC/DCAB CYCLE)	Indicates SDRAM DEAC or DCAB cycle
(SDRAM ACTV CYCLE)	Indicates SDRAM ACTV cycle
(FLUSH)	Indicates a cycle was fetched but not executed
(EXTENSION)	Indicates an extension to the preceding instruction opcode
(ASYNC READ CYCLE)	Indicates ASYNC memory READ cycle
(SBSRAM READ CYCLE)	Indicates SBSRAM READ cycle
(SDRAM READ CYCLE)	Indicates SDRAM READ cycle
(SBSRAM WRITE CYCLE)	Indicates SBSRAM WRITE cycle
(ASYNC WRITE CYCLE)	Indicates ASYNC WRITE cycle
(SDRAM WRITE CYCLE)	Indicates SDRAM WRITE cycle
(SBSRAM MRS CYCLE)	Indicates SDRAM MRS cycle
(UNKNOWN CYCLE)	Indicates a combination of control bits are unexpected or unrecognized

The external address bus has 19 lines EA21:EA2 lines for EMIF (External Memory Interface). However, the address internal to the processor are 32 bits. This 32 bit address is calculated based on Byte Enables, Chip Enables (Memory Space Enables) and user inputs. The Data bus has 32 lines ED31:ED0

Figure 2–7 shows an example of a Hardware display.

Sample	C6211 Address	C6211 Data	C6211 Mnemonics	C6211 Control	Timestamp
300	80000070	02840224	LDB.D1 *+A1[0t],A5	11111	10.000 ns
301	80000074	03000244	LDH.D1 *+A0[0t],A6	11111	10.000 ns
302	80000078	03880264	LDW.D1 *+A2[0t],A7	11111	10.500 ns
303	8000007C	029CAC80	MPY .M1 A5,A7,A5	11111	9.500 ns
307	80000080	029CAF82	MPYU .M2 B5,B7,B5	11111	270.500 ns
308	80000084	000000FA	SUB.L2 B0,B0,B0	SDREAD/SBREAD	9.500 ns
309	80000088	30000392	[!B0] B.S2 0x8000009C	11111	10.500 ns
310	8000008C	029CBE80	(FLUSH)	11111	9.500 ns
311	80000090	06A00234	(FLUSH)	11111	10.500 ns
312	80000094	07240254	(FLUSH)	11111	9.500 ns
313	80000098	07A80274	(FLUSH)	11111	10.500 ns
314	8000009C	029CAF82	(FLUSH)	11111	9.500 ns
318	800000A0	029CBE80	(FLUSH)	11111	280.000 ns
319	800000A4	018821F8	(FLUSH)	SDREAD/SBREAD	10.000 ns
320	800000A8	033DCDF8	(FLUSH)	11111	10.000 ns
321	800000AC	00082DE2	(FLUSH)	11111	10.000 ns
322	800000B0	0280081A	(FLUSH)	11111	10.000 ns
323	800000B4	0525EFD8	(FLUSH)	11111	10.500 ns
324	800000B8	041A48D8	(FLUSH)	11111	9.500 ns
325	800000BC	00010000	(FLUSH)	11111	10.500 ns
330	80000108	AAAAAAAA	(SDRAM READ CYCLE)	11111	240.000 ns
335	80000204	AAAAAAAA	(SDRAM READ CYCLE)	11111	249.500 ns
336	--------	--------	(SDRAM DEAC/DCAB CYCLE)	SDRAM_DCAB/DEAC	200.000 ns
337	00000000	--------	(SDRAM ACTV CYCLE)	SDRAM_ACTV	20.000 ns
341	80000408	AAAAAAAA	(SDRAM READ CYCLE)	11111	60.000 ns
342	--------	--------	(SDRAM DEAC/DCAB CYCLE)	SDRAM_DCAB/DEAC	210.500 ns
343	00000000	--------	(SDRAM ACTV CYCLE)	SDRAM_ACTV	20.000 ns
346	80000080	029CAF82	(FLUSH)	11111	50.000 ns
347	80000084	000000FA	(FLUSH)	SDREAD/SBREAD	10.000 ns
348	80000088	30000392	(FLUSH)	11111	9.500 ns
349	8000008C	029CBE80	(FLUSH)	11111	10.500 ns
350	80000090	06A00234	(FLUSH)	11111	9.500 ns
351	80000094	07240254	(FLUSH)	11111	10.500 ns
352	80000098	07A80274	(FLUSH)	11111	9.500 ns
353	8000009C	029CAF82	MPYU .M2 B5,B7,B5	11111	10.500 ns
357	800000A0	029CBE80	MPYUS .M1X A5,B7,A5	11111	220.000 ns
358	800000A4	018821F8	SSUB.L1 A1,A2,A3	SDREAD/SBREAD	9.500 ns

Figure 2–7: Hardware display format

Software Display Format

The Software display format displays only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but they will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format displays only the first fetch of instructions that cause a branch in the addressing and special cycles to change the flow of control.

Instructions that generate a change in the flow of control in the C6211/C6711 microprocessor are as follows:

B IRP B disp B NRP B reg

Subroutine Display Format

The Subroutine display format displays only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the C6211/C6711 microprocessor are as follows:

B IRP B NRP

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

Optional Display Selections

You can make optional selections for acquired disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

Show:	Hardware	(default)
	Software	
	Control Flow	
	Subroutine	
Highlight:	Software	(default)
	Control Flow	
	Subroutine	
	None	
Disasm Across Gaps:	Yes (default)	
	No	

Micro Specific Fields

Endian Mode. This field allows the user to indicate a C6211 processor configuration for viewing data from memory. The following selections will be available in the following order.

Little Endian	(default)
Big Endian	

The C6211 Processor has a single Memory Map. This memory map has four memory CE0,CE1,CE2,CE3 where user can read and write. The C6211/C6711 support can have three types of memories, ASYNC, SDRAM, SBSRAM. Any of these memory types can be allotted to any of the Memory spaces. So the following user inputs are required to know which memory is allotted to which memory spaces.

CE0 Space control. The user needs to enter the C6211 CE0 Space control Register's value. This field gives the memory type and the buswidth of that particular memory.

FFFFFF30	(default)

CE1 space control. The user needs to enter the C6211 CE1 Space control Register's value. This field gives the memory type and the buswidth of that particular memory.

FFFFFF23 (default)

CE2 space control. The user needs to enter the C6211 CE2 Space control Register's value. This field gives the memory type and the buswidth of that particular memory.

FFFFFF23 (default)

CE3 Space control. The user needs to enter the C6211 CE3 Space control Register's value. This field gives the memory type and the buswidth of that particular memory.

FFFFFF23 (default)

SDRAM Control Register. The user needs to enter the C6211 SDRAM Control register value. This gives the Row and Column address pins which are required for address calculation.

06117000 (default)

SDRAM Read Latency. The user needs to enter the CAS latency of SDRAM Read cycle.

Three (default)

CE0 START ADDR. The user needs to enter the Start address of the CE0 address space for the board.

80000000 (default)

CE1 START ADDR. The user needs to enter the Start address of the CE1 address space for the board.

90000000 (default)

CE2 START ADDR. The user needs to enter the Start address of the CE2 address space for the board.

A0000000 (default)

CE3 START ADDR. The user needs to enter the Start address of the CE3 address space for the board.

B0000000 (default)

SDRAM ADDR Configuration Field. The following Table 2–9 lists the common configuration of SDRAM that are fully supported by C6211/C6711 EMIF. The column *SDRAM Address configuration* lists numbers 1 through 11. The user must choose one of these numbers for the appropriate SDRAM Memory configuration on their board. The default value in in the SDRAM ADDR configuration field is 1. For the TI C6211 DSK kit, the C6211/C6711 support uses 0x3 in the SDRAM ADDR Configuration Field.

Table 2–9: C6211/C6711 Compatible SDRAM Memory Configuration

SDRAM size	Banks	Width	Depth	Max Devices/ CE	Address-able space (MBytes)		Column Address	Row Address	Bank Select	Pre-change	SDRAM Address configu-ration
16 Mbit	2	x4	2M	8	16M	SDRAM EMIF	A9 – A0 EA11 – EA2	A10 – A0 EA12 – EA2	A11 EA13	A10 EA12	1
	2	x8	1M	4	8M	SDRAM EMIF	A8 – A0 EA10 – EA2	A10 – A0 EA12 – EA2	A11 EA13	A10 EA12	2
	2	x16	512K	2	4M	SDRAM EMIF	A7 – A0 EA9 – EA2	A10 – A0 EA12 – EA2	A11 EA13	A10 EA12	3
64 Mbit	4	x4	4M	8	64M	SDRAM EMIF	A9 – A0 EA11 – EA2	A11 – A0 EA13 – EA2	A13–A12 EA15–EA14	A10 EA12	4
	4	x8	2M	4	32M	SDRAM EMIF	A8– A0 EA10 – EA2	A11 – A0 EA13 – EA2	A13–A12 EA15–EA14	A10 EA12	5
	4	x16	1M	2	16M	SDRAM EMIF	A7 – A0 EA9 – EA2	A11 – A0 EA13 – EA2	A13–A12 EA15–EA14	A10 EA12	6
	4	x32	512K	1	8M	SDRAM EMIF	A7 – A0 EA9 – EA2	A10 – A0 EA12 – EA2	A12–A11 EA14–EA13	A10 EA12	7
128 Mbit	4	x8	4M	4	64M	SDRAM EMIF	A9 – A0 EA11 – EA2	A11 – A0 EA13 – EA2	A13–A12 EA15–EA14	A10 EA12	8
	4	x16	2M	2	32M	SDRAM EMIF	A8 – A0 EA10 – EA2	A11– A0 EA13 – EA2	A13–A12 EA15–EA14	A10 EA12	9
256 Mbit	4	x8	8M	4	128M	SDRAM EMIF	A9 – A0 EA11 – EA2	A12 – A0 EA14 – EA2	A14–A13 EA16–EA15	A10 EA12	10
	4	x16	4M	2	64M	SDRAM EMIF	A8– A0 EA10 – EA2	A12– A0 EA14 – EA2	A14–A13 EA16–EA15	A10 EA12	11

The following user input fields for the C6211/C6711 support has a 256 word size Interrupt Service Table (IST). The IST is a table of fetch packets that contain code for servicing each of the Interrupts. The IST contains 16 fetch packets. Each Interrupt Service Routine is 32 bytes. The RESET has the Highest priority, NMI the second highest, and the lowest priority Interrupts are INT4 to INT15. The reset fetch packet must be located at address 0, but the rest of the interrupts, NMI and INT4–INT15, can be relocated anywhere within the IST (256 word boundary). Also, this IST can be relocated to any address location.

NOTE*. Since there are no Interrupt acknowledge signals and signals which tell which interrupt is being serviced, the user must enter the start address where the Service-Routine-Fetch packets are located.*

NMI_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address, of the NonMaskable Interrupt-Service-Routine Fetch Packet in the Interrupt Service Table.

00000020 (default)

INT4_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address, of the external interrupt EXT_INT4 Service-Routine-Fetch Packet in the Interrupt Service Table.

00000080 (default)

INT5_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address, of the external interrupt EXT_INT5 Service-Routine-Fetch Packet in the Interrupt Service Table.

000000A0 (default)

INT6_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address, of the external interrupt EXT_INT6 Service-Routine-Fetch Packet in the Interrupt Service Table.

000000C0 (default)

INT7_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address, of the external interrupt EXT_INT7 Service-Routine-Fetch Packet in the Interrupt Service Table.

000000E0 (default)

INT8_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address, of the external interrupt EXT_INT8 Service-Routine-Fetch Packet in the Interrupt Service Table.

00000100 (default)

INT9_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address, of the external interrupt EXT_INT9 Service-Routine-Fetch Packet in the Interrupt Service Table.

00000120 (default)

INT10_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address, of the external interrupt EXT_INT10 Service-Routine-Fetch Packet in the Interrupt Service Table.

00000140 (default)

INT11_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address of the external interrupt EXT_INT11 Service-Routine-Fetch Packet in the Interrupt Service Table.

00000160 (default)

INT12_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address of the external interrupt EXT_INT12 Service-Routine-Fetch Packet in the Interrupt Service Table.

00000180 (default)

INT13_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address of the external interrupt EXT_INT13 Service-Routine-Fetch Packet in the Interrupt Service Table.

000001A0 (default)

INT14_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address of the external interrupt EXT_INT14 Service-Routine-Fetch Packet in the Interrupt Service Table.

000001C0 (default)

INT15_FP_ADDR. The user needs to enter the 32 bit physical address; for example, Start Address of the external interrupt EXT_INT15 Service-Routine-Fetch Packet in the Interrupt Service Table.

000001E0 (default)

Marking Cycles

The TMS711 320C6211/C6711support allows marks to be placed by using the Mark Opcode button. The Mark Opcode will always be available. If the sample being marked is not an Address cycle or Data cycle of the potential bus master, the Mark Opcode selections will be replaced by a note indicating that "An Opcode Mark cannot be placed at the selected data sample."

When a cycle is marked, this character >> is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked by using the Undo Mark selection, which will remove this character >>. If more than one set of sequences are marked, then the user can undo the marks by using the "Remove all Marks" option.

The following cycle marks will be available:

- Reads can be marked as Opcode, Fetch, or Flash
- Fetch can be marked as Read or Flush
- Flush can be marked as Fetch or Opcode

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your C6211/C6711 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your system under test.

Specifications

Specifications

This chapter contains information regarding the specifications of the TMS711 320C6211/C6711 microprocessor support.

Specification Tables

Tables 3–1 and 3–2 list the electrical requirements the system under test must produce for the TMS711 320C6211/C6711 support to acquire correct data.

Table 3–1: C6211 Electrical specifications

Characteristics	Requirements
System under test clock rate	
Maximum specified clock rate:	
ASYNC memory	100 MHz
SBSRAM memory	100 MHz
SDRAM memory	100 MHz
Tested clock rate*	100 MHz
Minimum setup time required †	2.5 ns
Minimum hold time required †	0 ns

*** Please contact your Tektronix Sales Representative for current information on the tested clock rate.**

† Logic analyzer setup times are estimated for all signals for the supported memory cycles. However, you can change both the setup and hold times.

Table 3–2: C6711 Electrical Specifications

Characteristics	Requirements
Sytem under test clock rate	
Maximum specified clock rate:	
ASYNC memory	100 MHz
SBSRAM memory	100 MHz
SDRAM memory	100 MHz
Tested clock rate*	——
Minimum setup time required	2.5 ns
Minimum hold time required	0 ns

*** Please contact your Tektronix Sales Representative for current information on the tested clock rate.**

† **Logic analyzer setup times are estimated for all signals for the supported memory cycles. However, you can change both the setup and hold times.**

Replaceable Parts

Replaceable Parts

This section contains a list of the replaceable parts for the TMS711 320C6211/C6711 C6211/C6711 microprocessor support product.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071–0877–00			1	MANUAL, TECH: INSTRUCTIONS, C62XX, TMS711	TK2548	071–0877–00

Reference

Reference: Channel Groups

This section lists the Symbol table and the Channel group tables for disassembly and timing.

Symbol Table

Table 5–1 lists the name, bit pattern, and meaning for the symbols in the file C6211_Ctrl, the Control channel group symbol table.

Table 5–1: Control symbol table definitions

Symbol	Control group value RESET HOLDA~ AOE~/SDRAS~/SSOE~ ARE~/SDCAS~/SSADS~ AWE~/SDWE~/SSWE~
RESET	0 X X X X
HOLD_ACK	1 0 X X X
SDREAD/SBREAD	1 1 1 0 1
ASREAD	1 1 0 0 1
SDWRITE/SBWRTIE	1 1 1 0 0
ASWRITE	1 1 1 1 0
SDRAM_ACTV	1 1 0 1 1
SDRAM_DCAB/DEAC	1 1 0 1 0
SDRAM_MRS	1 1 0 0 0

Channel Assignments

Channel assignments listed in Tables 5–2 through 5–4 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are listed starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- An Tilde symbol (~) following a signal name indicates an active low signal.
- An equals symbol (=) following a signal name indicates that it is double probed.
- The module in the lower-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

  The portable logic analyzer has the lower numbered slots on the top and the benchtop logic analyzer has the lower numbered slots on the left.

The channel assignment groups will be displayed in the following order:

Group name	Display radix
Address	Hexadecimal
Data	Hexadecimal
Mnemonic	None
Control	Symbolic
Async	Off
CEnable	Off
BEnable	Off
Misc	Off

Table 5–2 lists the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default the Address channel group assignments are displayed in hexadecimal.

Table 5–2: Address channel group assignments

Bit order	Section:channel	C6211/C6711 signal name
31	A3:7	NC
21	A2:5	NC
20	A2:4	NC
19	A2:3	EA21
18	A2:2	EA20
17	A2:1	EA19
16	A2:0	EA18
15	A1:7	EA17
14	A1:6	EA16
13	A1:5	EA15
12	A1:4	EA14
11	A1:3	EA13
10	A1:2	EA12
9	A1:1	EA11
8	A1:0	EA10
7	A0:7	EA9
6	A0:6	EA8
5	A0:5	EA7
4	A0:4	EA6
3	A0:3	EA5
2	A0:2	EA4
1	A0:1	EA3
0	A0:0	EA2

Table 5–3 lists the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default the Data channel group assignments are displayed in hexadecimal.

Table 5–3: Data channel group assignments

Bit order	Section:channel	C6211/C6711 signal name
31	D3:7	ED31
30	D3:6	ED30

Table 5–3: Data channel group assignments (cont.)

Bit order	Section:channel	C6211/C6711 signal name
29	D3:5	ED29
28	D3:4	ED28
27	D3:3	ED27
26	D3:2	ED26
25	D3:1	ED25
24	D3:0	ED24
23	D2:7	ED23
22	D2:6	ED22
21	D2:5	ED21
20	D2:4	ED20
19	D2:3	ED19
18	D2:2	ED18
17	D2:1	ED17
16	D2:0	ED16
15	D1:7	ED15
14	D1:6	ED14
13	D1:5	ED13
12	D1:4	ED12
11	D1:3	ED11
10	D1:2	ED10
9	D1:1	ED9
8	D1:0	ED8
7	D0:7	ED7
6	D0:6	ED6
5	D0:5	ED5
4	D0:4	ED4
3	D0:3	ED3
2	D0:2	ED2
1	D0:1	ED1
0	D0:0	ED0

Table 5–4 lists the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. The default radix of the Control group is SYMBOLIC on the logic analyzer. The symbol table file name is C6211_Ctrl on the logic analyzer.

Table 5–4: Control channel group assignments

Bit order	Section:channel	C6211/C6711 signal name
4	C2:1	AOE~/SDRAS~/SSOE~
3	C2:0	AWE~/SDWE~/SSWE~
2	C2:2	ARE~/SDCAS~/SSADS~
1	C3:5	HOLDA~
0	C3:6	RESET~

By default Table 5–5 Async channel group assignments are not displayed.

Table 5–5: Async channel group assignments

Bit order	Section:channel	C6211/C6711 signal name
2	C2:1	AWE~/SDWE~/SSWE~
1	C2:0	ARE~/SDCAS~/SSADS~
0	C2:2	AOE~/SDRAS~/SSOE~

By default Table 5–6 CEnable channel group assignments are not displayed.

Table 5–6: CEnable channel group assignments

Bit order	Section:channel	C6211/C6711 signal name
3	C1:3	CE3~
2	C1:2	CE2~
1	C1:1	CE1~
0	C1:0	CE0~

By default Table 5–7 BEnable channel group assignments are not displayed.

Table 5–7: BEnable channel group assignments

Bit order	Section:channel	C6211/C6711 signal name
3	C1:7	BE3~
2	C1:6	BE2~

Table 5–7: BEnable channel group assignments (cont.)

Bit order	Section:channel	C6211/C6711 signal name
1	C1:5	BE1~
0	C1:4	BE0~

By default Table 5–8 Misc channel group assignments are not displayed.

Table 5–8: Misc channel group assignments

Bit order	Section:channel	C6211/C6711 signal name
0	Clock:3	ECLKOUT

Table 5–9 lists the probe section and clock and qualifier channel assignments. The clock probes are not part of any group.

Table 5–9: Clock and Qualifier channel assignments

Section:channel	C6211/C6711 signal name
CLK:3	ECLKOUT
C2:0	ARE~/SDCAS~/SSADS~
C2:1	AWE~/SDWE~/SSWE~
C2:2	AOE~/SDRAS~/SSOE~

Acquisition Setup. The TMS711 320C6211/C6711support affects the logic analyzer setup menus (and submenus) by modifying existing fields and adding micro-specific fields.

The TMS711 320C6211/C6711 support adds the selection C6211 to the Load Support Package dialog box, under the File pulldown menu. Once the C6211 support has been loaded, the Custom clocking mode selection in the module Setup menu is also enabled.

CPU To Mictor Connections

To probe the microprocessor you will need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-xx, for more information on mechanical specifications. Tables 5–10 through 5–16 list the CPU pin to Mictor pin connections.

Tektronix uses a counterclockwise pin assignment. Pin-1 is located at the top left, and pin-2 is located directly below it. Pin-20 is located on the bottom right, and pin-21 is located directly above it.

AMP uses an odd side-even side pin assignment. Pin-1 is located at the top left, and pin-3 is located directly below it. Pin-2 is located on the top right, and pin-4 is located directly below it (see Figure 5–1).

NOTE. *When designing Mictor connectors into your system under test, always follow the Tektronix pin assignment.*

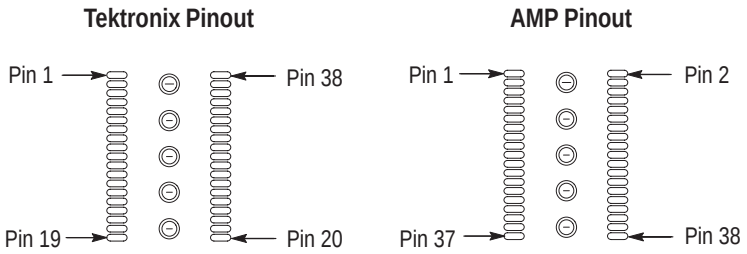


Figure 5–1: Pin assignments for a Mictor connector (component side)

NOTE. *To protect the CPU and the inputs of the module, it is recommended that a 180 Ω resistor is connected in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be within 1/2 inch of the ball pad of the CPU.*

Table 5–10: CPU to Mictor connections for Mictor A pins

Logic analyzer channel	C6211/C6711 signal name	AMP Mictor A pin number	Tektronix Mictor A pin number
A0:0	EA2	A38	A20
A0:1	EA3	A36	A21
A0:2	EA4	A34	A22

Table 5–10: CPU to Mictor connections for Mictor A pins (cont.)

Logic analyzer channel	C6211/C6711 signal name	AMP Mictor A pin number	Tektronix Mictor A pin number
A0:3	EA5	A32	A23
A0:4	EA6	A30	A24
A0:5	EA7	A28	A25
A0:6	EA8	A26	A26
A0:7	EA9	A24	A27
A1:0	EA10	A22	A28
A1:1	EA11	A20	A29
A1:2	EA12	A18	A30
A1:3	EA13	A16	A31
A1:4	EA14	A14	A32
A1:5	EA15	A12	A33
A1:6	EA16	A10	A34
A1:7	EA17	A8	A35
A2:0	EA18	A37	A19
A2:1	EA19	A35	A18
A2:2	EA20	A33	A17
A2:3	EA21	A31	A16
A2:4	NC	A29	A15
A2:5	NC	A27	A14
A2:6	NC	A25	A13
A2:7	NC	A23	A12
A3:0	NC	A21	A11
A3:1	NC	A19	A10
A3:2	NC	A17	A9
A3:3	NC	A15	A8
A3:4	NC	A13	A7
A3:5	NC	A11	A6
A3:6	NC	A9	A5
A3:7	NC	A7	A4

Table 5–11: CPU to Mictor connections for Mictor D pins

LA channel	C6211/C6711 signal name	AMP Mictor D pin number	Tektronix Mictor D pin number
D0:0	ED0	D38	D20
D0:1	ED1	D36	D21
D0:2	ED2	D34	D22
D0:3	ED3	D32	D23
D0:4	ED4	D30	D24
D0:5	ED5	D28	D25
D0:6	ED6	D26	D26
D0:7	ED7	D24	D27
D1:0	ED8	D22	D28
D1:1	ED9	D20	D29
D1:2	ED10	D18	D30
D1:3	ED11	D16	D31
D1:4	ED12	D14	D32
D1:5	ED13	D12	D33
D1:6	ED14	D10	D34
D1:7	ED15	D8	D35
D2:0	ED16	D37	D19
D2:1	ED17	D35	D18
D2:2	ED18	D33	D17
D2:3	ED19	D31	D16
D2:4	ED20	D29	D15
D2:5	ED21	D27	D14
D2:6	ED22	D25	D13
D2:7	ED23	D23	D12
D3:0	ED24	D21	D11
D3:1	ED25	D19	D10
D3:2	ED26	D17	D9
D3:3	ED27	D15	D8
D3:4	ED28	D13	D7
D3:5	ED29	D11	D6

Table 5–11: CPU to Mictor connections for Mictor D pins (cont.)

LA channel	C6211/C6711 signal name	AMP Mictor D pin number	Tektronix Mictor D pin number
D3:6	ED30	D9	D5
D3:7	ED31	D7	D4

Table 5–12: CPU to Mictor connections for Mictor C pins

LA channel	C6211/C6711 signal name	AMP Mictor C pin number	Tektronix Mictor C pin number
C2:0	ARE~/SDCAS~/SSADS~	C37	C19
C2:1	AWE~/SDWE~/SSWE~	C35	C18
C2:2	AOE~/SDRAS~/SSOE~	C33	C17
C3:5	HOLDA~	C11	C6
C3:6	RESET~	C9	C5

Table 5–13: CPU to Mictor connections for CEnable

LA channel	C6211/C6711 signal name	AMP Mictor C pin number	Tektronix Mictor C pin number
C1:0	CE0~	C22	C28
C1:1	CE1~	C20	C29
C1:2	CE2~	C18	C30
C1:3	CE3~	C16	C31

Table 5–14: CPU to Mictor connections for BEnable

LA channel	C6211/C6711 signal name	AMP Mictor C pin number	Tektronix Mictor C pin number
C1:4	BE0~	C14	C32
C1:5	BE1~	C12	C33
C1:6	BE2~	C10	C34
C1:7	BE3~	C8	C35

Table 5–15: CPU to Mictor connections for Misc

LA channel	C6211/C6711 signal name	AMP Mictor C pin number	Tektronix Mictor C pin number
Clock:3	ECLKOUT	C2	C03

Table 5–16: CPU to Mictor connections for clock and qualifiers

LA channel	C6211/C6711 signal name	AMP Mictor C pin number	Tektronix Mictor C pin number
CLK:3	ECLKOUT	C2	C03
C2:0	ARE~/SDCAS~/SSADS~ (Qualifier)	C37	C19
C2:1	AWE~/SDWE~/SSWE~ (Qualifier)	C35	C18
C2:2	AOE~/SDRAS~/SSOE~ (Qualifier)	C33	C17

Index

Index